WHAT IS CLAIMED IS:

1. A disk controller comprising:

a channel adapter having a connection interface to a host computer or a disk drive;

a memory adapter for temporarily storing data to be transferred between said host computer and said disk drive;

a processor adapter for controlling operations of said channel adapter and said memory adapter; and

a switch adapter for configuring an inner network by interconnecting said channel adapter, said memory adapter and said processor adapter,

wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a DMA controller for performing a communication protocol control of said inner network; and

packet multiplex communication is performed among said DMA controllers provided in said adapters.

2. The disk controller according to claim 1, wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a plurality of DMA controllers and one or more data link engines; and

said plurality of DMA controllers share said data link engine and perform DMA transfer at the same

time via said data link engine.

3. The disk controller according to claim 2, wherein:

said DMA controller includes a plurality of reception FIFO buffers and a plurality of transmission FIFO buffers; and

contention of reception data is arbitrated among said plurality of reception FIFO buffers, and contention of transmission data is arbitrated among said plurality of transmission FIFO buffers.

4. The disk controller according to claim 1, wherein:

said DMA controller includes a plurality of reception FIFO buffers and a plurality of transmission FIFO buffers; and

contention of reception data is arbitrated among said plurality of reception FIFO buffers, and contention of transmission data is arbitrated among said plurality of transmission FIFO buffers.

5. The disk controller according to claim 1, wherein:

said DMA controller includes a reception FIFO buffer and a transmission FIFO buffer; and

contention of reception data is arbitrated among respective reception FIFO buffers belonging to a plurality of DMA controllers, and contention of transmission data is arbitrated among respective transmission FIFO buffers belonging to a plurality of

DMA controllers.

6. The disk controller according to claim 2, wherein:

said DMA controller includes a reception FIFO buffer and a transmission FIFO buffer; and

contention of reception data is arbitrated among respective reception FIFO buffers belonging to a plurality of DMA controllers, and contention of transmission data is arbitrated among respective transmission FIFO buffers belonging to a plurality of DMA controllers.

7. A disk controller comprising:

a channel adapter having a connection interface to a host computer or a disk drive;

a memory adapter for temporarily storing data to be transferred between said host computer and said disk drive;

a processor adapter for controlling operations of said channel adapter and said memory adapter; and

a switch adapter for configuring an inner network by interconnecting said channel adapter, said memory adapter and said processor adapter,

wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a plurality of DMA controllers for performing a communication protocol control of said inner network,

and one or more data link engines shared by said DMA controllers;

said DMA controller include a plurality of reception FIFO buffers and a plurality of transmission FIFO buffers, one data link engine being made in correspondence with a plurality of buffers;

contention of reception data is arbitrated among respective reception FIFO buffers belonging to a plurality of DMA controllers, and contention of transmission data is arbitrated among respective transmission FIFO buffers belonging to a plurality of DMA controllers, to thereby set a priority order of a plurality of buffers; and

a control system inner network and a data system inner network are mixed in one data link engine, and packet multiplex communication is performed among said DMA controllers provided in said adapters.

8. A disk controller comprising:

a channel adapter having a connection interface to a host computer or a disk drive;

a memory adapter for temporarily storing data to be transferred between said host computer and said disk drive;

a processor adapter for controlling operations of said channel adapter and said memory adapter; and

a switch adapter for configuring an inner network by interconnecting said channel adapter, said

memory adapter and said processor adapter,

wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a DMA controller for performing a communication protocol control of said inner network;

a packet to be transferred among said DMA controllers provided in said adapters has an address field for designating a targeting DMA controller, an address field for designating an initiating DMA controller and a DMA sequence field for managing a transfer order when one DMA transfer is divided into a plurality of packets; and

said DMA sequence field has a task ID unique to one DMA transfer.

9. The disk controller according to claim 8, wherein a packet to be transferred among said DMA controllers provided in said adapters has a first address for designating a relay DMA controller of said packet, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers.

10. The disk controller according to claim 9, wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a plurality of DMA controllers and one or more data link engines;

a packet to be transferred among said DMA controllers provided in said adapters comprises a routing field containing control information for said data link engine, a command field containing control information for said DMA controller and a data field containing other data; and

said routing field includes a routing field error check code for checking a transfer error in said routing field, said command field includes a command field error check code for checking a transfer error in said command field, and said data field includes a data field error check code for checking a transfer error in said data field.

11. The disk controller according to claim 8, wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a plurality of DMA controllers and one or more data link engines;

a packet to be transferred among said DMA controllers provided in said adapters comprises a routing field containing control information for said data link engine, a command field containing control information for said DMA controller and a data field containing other data; and

said routing field includes a routing field error check code for checking a transfer error in said routing field, said command field includes a command

field error check code for checking a transfer error in said command field, and said data field includes a data field error check code for checking a transfer error in said data field.

12. The disk controller according to claim 11, wherein:

DMA sub-transfer is performed from a DMA controller designated by said initiating address field to a DMA controller designated by said targeting address field;

said DMA controller designated by said targeting address field returns a completion sub-status corresponding to said DMA sub-transfer to said DMA controller designated by said initiating address field;

said completion sub-status includes information of said DMA sequence field contained in said DMA sub-transfer; and

said DMA controller designated by said initiating address field confirms the information of said DMA sequence field contained in said completion sub-status to thereby confirm a transfer sequence of said DMA sub-transfer.

13. The disk controller according to claim 8, wherein:

DMA sub-transfer is performed from a DMA controller designated by said initiating address field to a DMA controller designated by said targeting address field;

said DMA controller designated by said targeting address field returns a completion sub-status corresponding to said DMA sub-transfer to said DMA controller designated by said initiating address field;

said completion sub-status includes information of said DMA sequence field contained in said DMA sub-transfer; and

said DMA controller designated by said initiating address field confirms the information of said DMA sequence field contained in said completion sub-status to thereby confirm a transfer sequence of said DMA sub-transfer.

14. The disk controller according to claim 9, wherein:

DMA sub-transfer is performed from a DMA controller designated by said initiating address field to a DMA controller designated by said targeting address field;

said DMA controller designated by said targeting address field returns a completion sub-status corresponding to said DMA sub-transfer to said DMA controller designated by said initiating address field;

said completion sub-status includes information of said DMA sequence field contained in said DMA sub-transfer; and

said DMA controller designated by said initiating address field confirms the information of said DMA sequence field contained in said completion

sub-status to thereby confirm a transfer sequence of said DMA sub-transfer.

15. The disk controller according to claim 14, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a packet which has said third address in said targeting address field and contains said transfer data.

16. The disk controller according to claim 8, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a packet which has said third address in said targeting address field and contains said transfer data.

17. The disk controller according to claim 9, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a packet which has said third address in said targeting address field and contains said transfer data.

18. The disk controller according to claim 10, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a packet which has said third address in said targeting address field and contains said transfer data.

19. The disk controller according to claim 8, wherein:

a packet to be transferred among said DMA controllers provided in said adapters comprises a header field containing packet control information and a data field containing other data;

said header field includes a header field error check code for checking a transfer error in said header field, and said data field includes a data field error check code for checking a transfer error in said data field; and

said DMA controller in said switch adapter passes only a packet having a correct header field error check code.

20. The disk controller according to claim 9, wherein:

a packet to be transferred among said DMA controllers provided in said adapters comprises a header field containing packet control information and a data field containing other data;

said header field includes a header field error check code for checking a transfer error in said header field, and said data field includes a data field error check code for checking a transfer error in said data field; and

said DMA controller in said switch adapter passes only a packet having a correct header field error check code.

21. The disk controller according to claim 1, wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a plurality of DMA controllers and a plurality of data link engines; and

when said DMA controller performs DMA transfer via said data link engine, DMA transfer is performed via a same data link engine during one DMA transfer.

22. A disk controller having one disk controller and another disk controller, wherein:

said one disk controller comprises:

one channel adapter having a connection interface to a host computer or a disk drive;

one memory adapter for temporarily storing data to be transferred between said host computer and said disk drive;

one processor adapter for controlling operations of said one channel adapter and said one memory adapter; and

one switch adapter for configuring an inner network by interconnecting said one channel adapter, said one memory adapter and said one processor adapter,

wherein:

said one channel adapter, said one memory adapter, said one processor adapter and said one switch adapter each include a DMA controller for performing a communication protocol control of said inner network; and

packet multiplex communication is performed among said DMA controllers provided in said adapters, and

wherein said other disk controller comprises adapters having similar structures to structures of said one channel adapter, said one memory adapter, said one processor adapter and said one switch adapter of said one disk controller;

said one switch adapter is connected to each of said one adapters and to each of said other adapters; and

said other switch adapter is connected to each of said other adapters and to each of said one adapters.

23. The disk controller according to claim 22, wherein expansion ports of said one switch adapter and/or said other switch adapter are connected to expansion ports of another switch adapter.

24. A disk controller comprising:

a channel adapter having a connection interface to a host computer or a disk drive;

a memory adapter for temporarily storing data to be transferred between said host computer and said disk drive;

a processor adapter for controlling operations of said channel adapter and said memory adapter; and

a switch adapter for configuring an inner

network by interconnecting said channel adapter, said memory adapter and said processor adapter,

wherein:

said channel adapter, said memory adapter, said processor adapter and said switch adapter each include a DMA controller for performing a communication protocol control of said inner network, and a data link engine for executing DMA transfer to and from said inner network; and

a packet to be transferred among said DMA controllers provided in said adapters comprises an address field for designating a targeting DMA controller, an address field for designating an initiating DMA controller and a DMA sequence field for managing a transfer sequence when one DMA transfer is distributed to a plurality of packets.